FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
10004543-1	09/777,202
APPLICANT: Brian William Hughes	
FILING DATE: 02/02/2001	GROUP

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	1A	6,141,779	10/31/2000	Hill et al.	714	710
	1B	5,255,227	10/19/1993	Heaffele	365	200
	1C	5,848,077	12/08/1998	Kamae et al.	371	53
	1D	6,000,047	10/07/1999	Kamae et al.	714	710
	1E	6,134,681	10/17/2000	Akamatsu et al.	714	710
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO
	1L							
	1M							
	1N							
	1O							
	1P							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	http://www.howstuffworks.com/ram.htm?printable=1 -- How Random Access Memory (RAM) Works, by Jeff Tyson (8 pages)
	1R	http://www.xtronics.com/memory/how_memory-works.htm -- How Memory Works, by Dr. Ah Clem Memory (11 pages)
	1S	http://www.pct chguid .com/03memory.htm -- Th Technology Guid (System M mory) (9 pages)

EXAMINER

DATE CONSIDERED 2/17/2004

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
10004543-1	09/777,202
APPLICANT: Brian William Hughes	
FILING DATE: 02/02/2001	GROUP

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	2A					
	2B					
	2C					
	2D					
	2E					
	2F					
	2G					
	2H					
	2I					
	2J					
	2K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO
	2L							
	2M							
	2N							
	2O							
	2P							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

2Q	http://www.eecs.harvard.edu/cs245/papers/Davidb.html -- Built-in Self Test of Dram Chips(5 pages)
2R	Processor-Based Built-In Self Test For Embedded DRAM by Jeffrey Dreibelbis, et al. IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, November, 1998 pp. 1731-1740
2S	March LR: A Test for Realistic Linked Faults, J.J. van de Goor, et al. 14th VLSI Test Symposium -- 1996 IEEE pp. 272-280

EXAMINER [signature] DATE CONSIDERED 2/10/2004

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
10004543-1	09/777,202
APPLICANT: Brian William Hughes	
FILING DATE: 02/02/2001	GROUP

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	3A					
	3B					
	3C					
	3D					
	3E					
	3F					
	3G					
	3H					
	3I					
	3J					
	3K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO
	3L							
	3M							
	3N							
	3O							
	3P							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	3Q	On-Wafer BIST of a 200-Gb/s Failed-Bit Search for 1-Gb DRAM, Satoru Tanoi, et al. IEEE Journal of Solid-State Circuits, Vol. 32, No. 11. November, 1997, pp.1735-1742
	3R	An Algortihm for Row-Column Self-Repair of RAMs and Its Implementation in the Alpha 21264, Dilip K. Bhavsar ITC International Test Conference Paper 12.3; IEEE 1999, pp. 311-318
	3S	

EXAMINER

DATE CONSIDERED 2/10/2004